Amendments To The Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-51 (canceled)

52. (new) A memory device comprising:

means for inputting a programming voltage;

means for inputting control signals indicative of an operational mode of said memory device;

means for determining from said control signals whether the program voltage is being input from an external interface or from an internal signal line of said memory device; and

means for preventing the program voltage from being sent to the external interface while allowing the program voltage to reach the programmable element if it is determined that the program voltage is being input from the internal signal line.

53. (new) The memory device of claim 52, further comprising means for passing the programming voltage to the signal line if it is determined that the program voltage is being input from the external interface.

54. (new) The memory device of claim 52, wherein said means for inputting the programming voltage comprises means for inputting the programming voltage from a bond pad of the memory device.

55. (new) The memory device of claim 52, wherein said means for inputting the programming voltage comprises inputting the programming voltage from a probe being applied directly to the signal line.

56. (new) A processor system comprising:

a processor; and

a memory device coupled to said processor, said memory device comprising:

means for inputting a programming voltage,

means for inputting control signals indicative of an operational mode of said memory device,

means for determining from said control signals whether the program voltage is being input from an external interface or from an internal signal line of said memory device, and

means for preventing the program voltage from being sent to the external interface while allowing the program voltage to reach the programmable

element if it is determined that the program voltage is being input from the internal signal line.

57. (new) The system of claim 56, wherein said memory device further comprises means for passing the programming voltage to the signal line if it is determined that the program voltage is being input from the external interface.

58. (new) The system of claim 56, wherein said means for inputting the programming voltage comprises means for inputting the programming voltage from a bond pad of the memory device.

59. (new) The system of claim 56, wherein said means for inputting the programming voltage comprises inputting the programming voltage from a probe being applied directly to the signal line.